# HamGeek HG61 Pro/HG63 Pro SDR
# User Manual

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# I. Product Overview

## 1.1 Product Overview

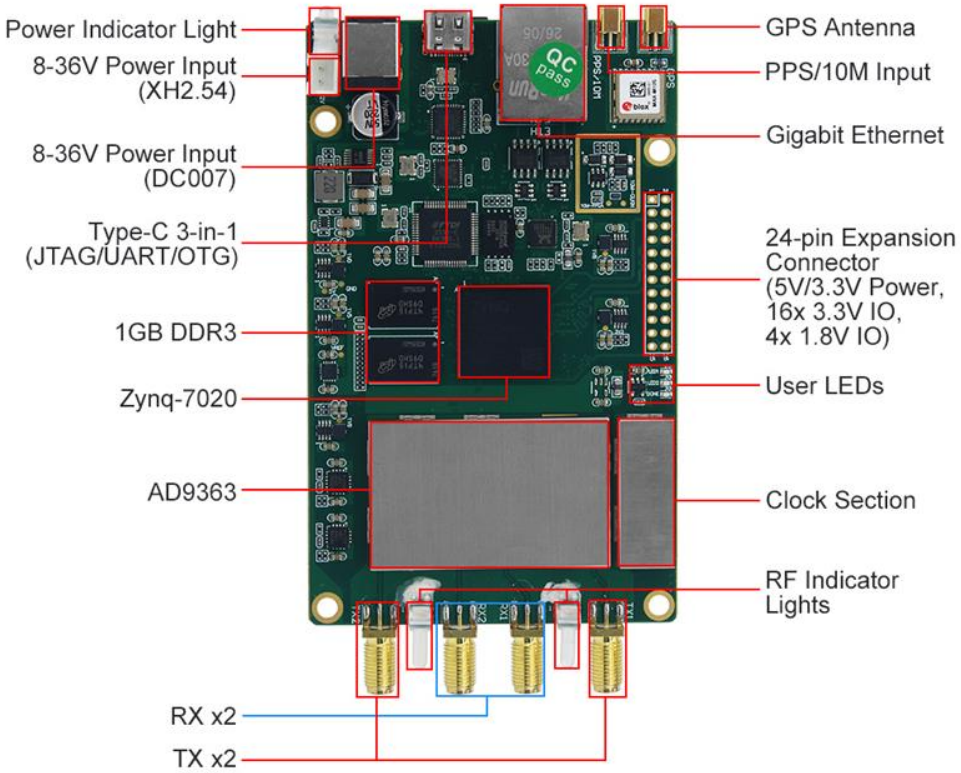
This article introduces the HamGeek HG61 Pro and HG63 Pro, two fully compatible hardware platforms that support direct software replacement. Both products are based on the XC7Z020-2CLG400I main controller and integrate ADI's AD9361/AD9363 RF transceiver chips as the core RF architecture.

The HG61 Pro is a ZYNQ7020-based platform equipped with the AD9361 RF chip, while the HG63 Pro is a ZYNQ7020-based platform equipped with the AD9363 RF chip. The main difference between the two products lies in the RF bandwidth capability, allowing users to select the appropriate model according to their specific application requirements.

The HG61 Pro/HG63 Pro integrates multiple RF and hardware interfaces, providing abundant resources, flexible connectivity, and ease of use. The following Product Function Block Diagram provides an overview of the internal resource architecture.

The PCBA board dimensions are 115mm x 70mm (4.53 inch x 2.76 inch), with a PCB thickness of 2.2mm. The optional customized enclosure measures 125mm x 75mm (4.92 inch x 2.95 inch). The enclosure also functions as a heat dissipation structure, ensuring stable and reliable operation.

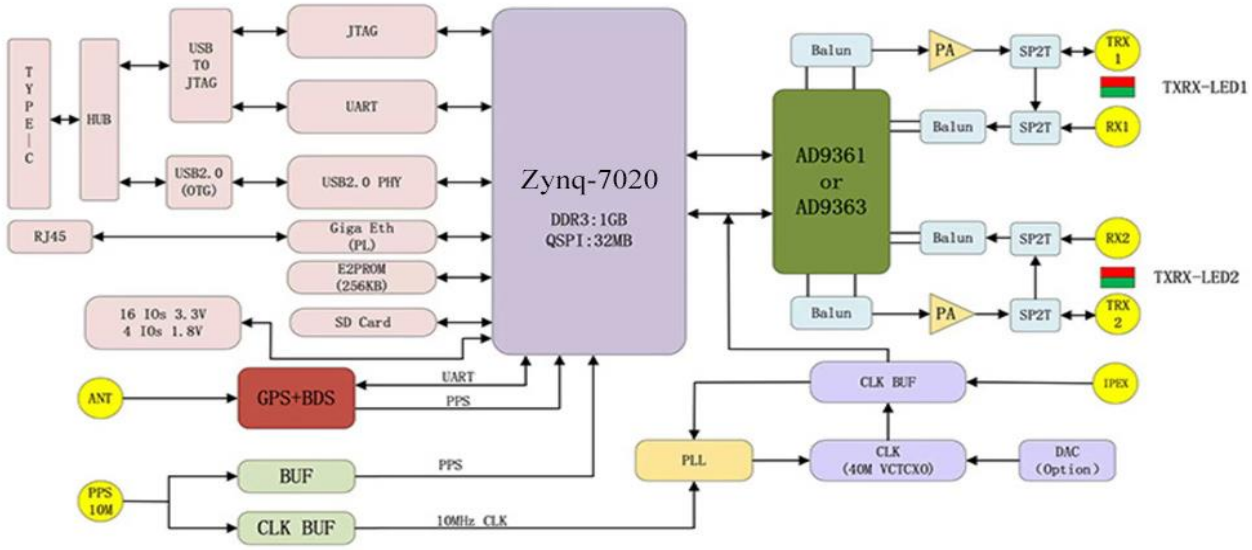
Designed according to industrial-grade standards, the products support an operating temperature range of -40° C to 85° C. They feature a 0.1ppm high-precision clock source, and all interfaces are equipped with electrostatic discharge (ESD) protection to improve reliability in demanding environments.




## 1.2 Product Function Block Diagram

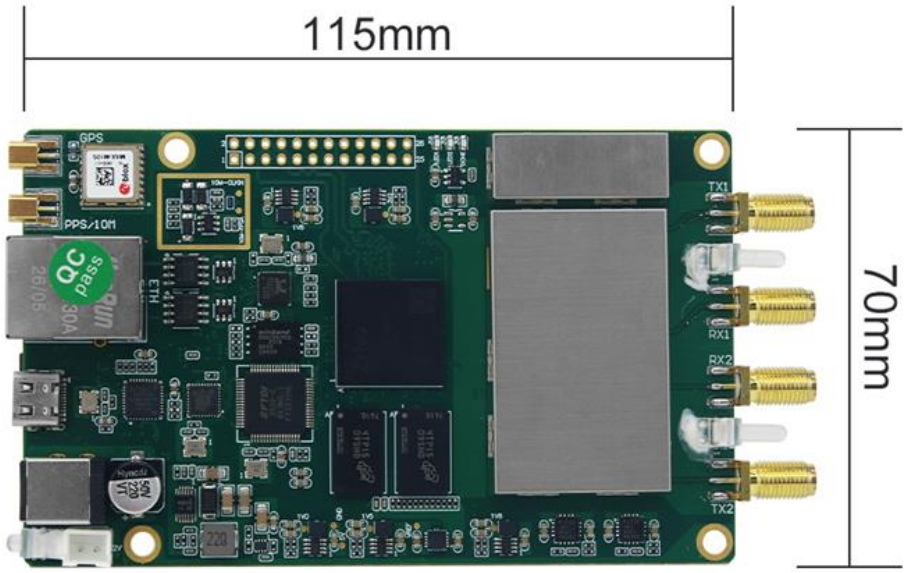
In this section, we will provide a detailed overview of the product configuration through the product block diagram and technical specifications, as shown below.

# Product Block Diagram




## 1.3 Product Dimensions

The PCBA board measures 115mm x 70mm (4.53 inch x 2.76 inch), and the customized enclosure measures 125mm x 75mm (4.92 inch x 2.95 inch).


115mm
70mm
GPS
PPS/10M
ETH
TX1
RX1
RX2
TX2


## II. Hardware Overview

### 2.1 HG61 Pro vs. HG63 Pro

The following table lists the key specifications of the HG61 Pro and HG63 Pro. The main difference between the two products is the selection of different RF chips. As a result, the two models feature different RF frequency ranges and signal bandwidth capabilities. Users can refer to the comparison table below to select the most suitable product according to their application requirements.

# Specifications

| Model | HG61 Pro | HG63 Pro |
|---|---|---|
| RF Chip | AD9361 | AD9363 |
| Frequency Range | 70M-6Ghz | 325M-3.8Ghz |
| Signal Bandwidth | 200K-56Mhz | 200K-20Mhz |
| Power Amplification | 2-Channel TX | |
| Processor | XC7Z020-2CLG400I | |
| Core Frequency | Dual-core Cortex-A9, 766MHz | |
| Logic Cells | 85K | |
| DDR3 | 1GB | |
| QSPI Flash | 256Mb | |
| EEPROM | 256Kb | |
| RF Clock Source | 40M VCTCXO (0.5PPM)/IPEX Input/External Input (Default: 40M VCTCXO) | |
| Gigabit Ethernet | 1 Channel | |
| USB OTG | 1 Channel | |
| UART | 1 Channel | |
| JTAG | 1 Channel | |
| SD Card | 1 Channel | |
| GPS | 1 Channel | |
| PPS/10MHz Input | 1 Channel | |
| Expansion IO | 16x 3.3V IO, 4x 1.8V IO | |
| Dimensions | Board only: 115mm x 70mm x 2.2mm; Enclosure case: 125mm x 75mm x 23mm | |
| Protection Level | Static electricity protection on all external interfaces; shield protection on clock and RF | |
| Power Supply | 8-36V Ultra-wide voltage supply (Limit: 50V) | |
| Operating Temperature | -40°C to 85°C | |

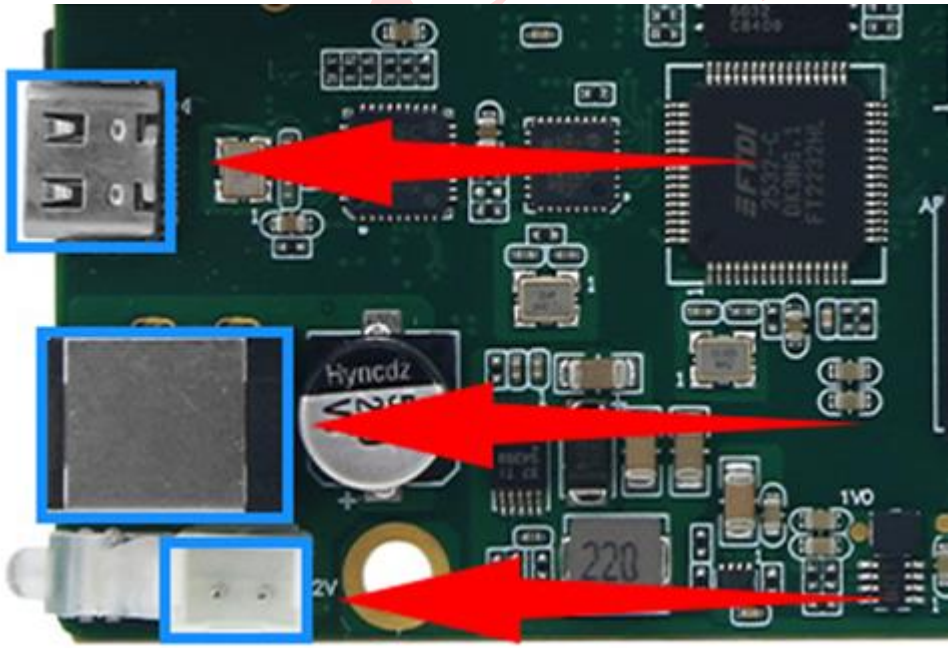
## 2.2 Power Supply

The product supports three power supply options: XH2.54 connector, Type-C interface, and DC007 interface. These three power supply methods provide flexible options for different application scenarios.

XH2.54 Interface:
When the product is integrated into a device, power can be supplied through the XH2.54 connector. The supported input voltage range is 8-36V/1A.

Type-C Interface:
The Type-C interface provides multiple functions. It can be used to power the board by connecting directly to a computer's USB port, providing a 5V power supply. In addition, it also serves as a communication interface, supporting JTAG and UART functions for convenient board programming, debugging, and development.

DC007 Interface:
The DC007 interface is connected in parallel with the XH2.54 power input, so only one of these two interfaces should be used at a time. However, the Type-C interface is designed with power compatibility, allowing it to be connected simultaneously with either XH2.54 or DC007 without causing power conflicts.




## 2.3 System Clock

The HG61 Pro/HG63 Pro provides a 33.33MHz clock input for the PS side. The input pin is assigned to PS_CLK_500. In addition, a 40MHz clock input is provided for the PL side through IO_L11P_SRCC_35 (Pin No. J16).

## 2.4 Global Reset

The HG61 Pro/HG63 Pro provides an nGST reset button located near the edge of the board for system reset operations. The reset signal is active low.

The nGST reset signal is connected to PS_POR_500 on the PS side and IO_12N_MRCC_34 (Pin No. U19) on the PL side, respectively.

## 2.5 Boot Mode Selection

The HG61 Pro/HG63 Pro supports three boot modes: JTAG, QSPI Flash, and SD Card. The boot mode can be selected using the onboard toggle switch. When the switch is set to the JTAG position, the board enters JTAG boot mode, allowing users to download programs and perform debugging through the JTAG interface. When the switch is set to the QSPI/SD position, the board enters QSPI Flash or SD Card boot mode. A special boot management design is implemented: when no SD card is detected, the system automatically boots from the QSPI Flash. When an SD card is inserted, the boot mode automatically switches to SD Card boot mode.

## 2.6 DDR3 Introduction

The PS side is equipped with two industrial-grade DDR3 memory chips, each with a capacity of 512MB, providing a total memory capacity of 1GB. The memory device model is MT41K256M16TW-107IT:P. The DDR3L pin assignment is predefined in the system configuration and can be used directly. Users can also refer to the demonstration projects provided by the manufacturer.

## 2.7 QSPI Flash Introduction

The HG61 Pro/HG63 Pro is equipped with a 256Mb QSPI Flash memory for storing boot files and user files.

| QSPI FLASH Pin | Pin Name | Pin Position |
|---|---|---|
| DATA0 | MIO2 | B8 |
| DATA1 | MIO3 | D6 |
| DATA2 | MIO4 | B7 |
| DATA3 | MIO5 | A6 |
| QSPI_CS | MIO1 | A7 |
| QSPI_CLK | MIO6 | A5 |

## 2.8 EEPROM Introduction

An EEPROM memory chip is reserved on the HG61 Pro/HG63 Pro, with a capacity of 256Kb. The

pin definitions are listed in the table below.

| E2PROM PIN | PIN Name | PIN Position |
|---|---|---|
| I2C_SCL | MIO10 | E9 |
| I2C_SDA | MIO11 | C6 |

## 2.9 PL Side Gigabit Ethernet

The Gigabit Ethernet chip is placed on the carrier board and connected to the Zynq processor through the PL side. The corresponding pin connections are shown in the table below. PHY Address: PHY_AD[2:0] = 010

| RMGII Signal | Pin Name | Pin Position |
|---|---|---|
| GPHY_GTX_CLK | IO_L3P_35 | E17 |
| GPHY_TXD0 | IO_L3N_35 | D18 |
| GPHY_TXD1 | IO_L4P_35 | D19 |
| GPHY_TXD2 | IO_L4N_35 | D20 |
| GPHY_TXD3 | IO_L5P_35 | E18 |
| GPHY_TX_EN | IO_L5N_35 | E19 |
| GPHY_RX_CLK | IO_L13P_MRCC_35 | H16 |
| GPHY_RXD0 | IO_L6P_35 | F16 |
| GPHY_RXD1 | IO_L6N_35 | F17 |
| GPHY_RXD2 | IO_L7P_35 | M19 |
| GPHY_RXD3 | IO_L7N_35 | M20 |
| GPHY_RX_DV | IO_L8P_35 | M17 |
| GPHY_MDC | IO_L2P_35 | B19 |
| GPHY_MDIO | IO_L2N_35 | A20 |

## 2.10 SD Card Interface

The SD card socket is located on the carrier board and connected to BANK 501 on the PS side of the Zynq processor. Since the I/O voltage level of BANK 501 is 1.8V, while the SD card interface operates at 3.3V, a TXS02612RTWR level translator is used for voltage level conversion.

The pin assignment and schematic diagram of the SD card interface are shown below. For detailed information, please refer to the schematic.

| SD Card Slot Interface | Pin Name | Pin Position |
|---|---|---|
| SD_CLK | MIO40 | D14 |
| SD_CMD | MIO41 | C17 |
| SD_DATA0 | MIO42 | E12 |
| SD_DATA1 | MIO43 | A9 |
| SD_DATA2 | MIO44 | F13 |
| SD_DATA3 | MIO45 | B15 |

## 2.11 USB-to-JTAG and UART

The HG61 Pro/HG63 Pro is designed with a USB-to-JTAG/UART interface. The JTAG interface is connected to the JTAG port of the host processor, while the UART interface is connected to the UART1 pin of the host processor. The UART pin assignment is shown in the table below. For detailed circuit information, please refer to the schematic.

| UART | Pin Name | Pin Position |
|---|---|---|
| UART1_TX | MIO12 | D9 |
| UART1_RX | MIO13 | E8 |

## 2.12 USB 2.0

The USB 2.0 interface chip is integrated on the HG61 Pro/HG63 Pro. The following table shows the connection relationship between the USB PHY and the main processor. For detailed information, please refer to the schematic.

| USB2.0 Signal | Pin Name | Pin Position |
|---|---|---|
| USBPHY_DATA0 | MIO32 | A14 |
| USBPHY_DATA1 | MIO33 | D15 |
| USBPHY_DATA2 | MIO34 | A12 |
| USBPHY_DATA3 | MIO35 | F12 |
| USBPHY_DATA4 | MIO28 | C16 |
| USBPHY_DATA5 | MIO37 | A10 |
| USBPHY_DATA6 | MIO38 | E13 |
| USBPHY_DATA7 | MIO39 | C18 |
| USBPHY_STP | MIO30 | C15 |
| USBPHY_NXT | MIO31 | E16 |
| USBPHY_DIR | MIO29 | C13 |
| USBPHY_CLKOUT | MIO36 | A11 |
| USB_nRSET | MIO48 | B12 |

## 2.13 AD9361 Introduction

The RF section of the product is based on ADI's AD9361 RF transceiver. This section provides a detailed introduction to the RF architecture, including the RF signal path, data interface, and clock system.

### * 2.13.1 RF Front-End Circuit

The RF front-end circuit consists of three main components: balun, amplifier, and RF switch. The balun provides a frequency bandwidth of 10MHz to 6GHz, covering the communication frequency range supported by the AD9361.

The amplifier operates over a frequency range of 50MHz to 6GHz, which also covers the AD9361 communication bandwidth. However, the gain flatness varies slightly across the operating frequency range. The detailed amplifier performance parameters at different frequency points are listed in the following table.

| FREQ | Gain | Isolation | Input Return Loss | Output Return Loss | Stability | | IP-3 Output | 1dB Comp. Output | Noise Figure |
|---|---|---|---|---|---|---|---|---|---|
| (MHz) | (dB) | (dB) | (dB) | (dB) | K | Measure | (dBm) | (dBm) | (dB) |
| 50.00 | 17.73 | 23.19 | 14.21 | 18.51 | 1.14 | 0.76 | 31.53 | 17.82 | 2.10 |
| 80.00 | 17.14 | 22.43 | 16.76 | 18.87 | 1.14 | 0.73 | 32.21 | 17.91 | 1.97 |
| 100.00 | 16.93 | 22.26 | 18.14 | 19.00 | 1.15 | 0.72 | 32.46 | 17.83 | 2.00 |
| 200.00 | 16.55 | 22.00 | 21.40 | 19.27 | 1.18 | 0.72 | 32.09 | 17.88 | 1.96 |
| 400.00 | 16.32 | 21.92 | 22.06 | 19.17 | 1.19 | 0.72 | 32.80 | 17.69 | 2.18 |
| 500.00 | 16.22 | 21.95 | 21.60 | 19.08 | 1.20 | 0.73 | 32.65 | 17.75 | 2.22 |
| 600.00 | 16.12 | 21.91 | 20.87 | 18.92 | 1.21 | 0.73 | 32.75 | 17.73 | 2.18 |
| 800.00 | 15.90 | 21.94 | 19.22 | 18.59 | 1.23 | 0.75 | 32.97 | 17.68 | 2.22 |
| 1000.00 | 15.63 | 21.95 | 17.75 | 18.27 | 1.24 | 0.77 | 32.35 | 17.74 | 2.14 |
| 1200.00 | 15.34 | 21.94 | 16.45 | 17.96 | 1.26 | 0.79 | 33.10 | 17.70 | 2.27 |
| 1400.00 | 15.03 | 21.96 | 15.29 | 17.73 | 1.29 | 0.81 | 33.34 | 17.71 | 2.28 |
| 1500.00 | 14.88 | 21.96 | 14.70 | 17.47 | 1.29 | 0.82 | 32.76 | 17.78 | 2.31 |
| 1600.00 | 14.70 | 21.96 | 14.37 | 17.59 | 1.31 | 0.83 | 33.06 | 17.69 | 2.35 |
| 1800.00 | 14.38 | 21.98 | 13.49 | 17.43 | 1.33 | 0.85 | 33.66 | 17.56 | 2.36 |
| 2000.00 | 14.04 | 21.97 | 12.88 | 17.64 | 1.36 | 0.87 | 33.23 | 17.81 | 2.39 |
| 2200.00 | 13.72 | 21.93 | 12.29 | 17.75 | 1.38 | 0.89 | 33.13 | 17.99 | 2.45 |
| 2400.00 | 13.42 | 21.90 | 11.83 | 17.77 | 1.40 | 0.91 | 33.38 | 17.82 | 2.44 |
| 2500.00 | 13.27 | 21.94 | 11.64 | 17.87 | 1.41 | 0.92 | 33.32 | 17.96 | 2.50 |
| 2600.00 | 13.13 | 21.94 | 11.46 | 17.91 | 1.43 | 0.93 | 33.58 | 17.80 | 2.61 |
| 2800.00 | 12.85 | 21.83 | 11.14 | 17.97 | 1.44 | 0.95 | 33.46 | 17.78 | 2.65 |
| 3000.00 | 12.57 | 21.81 | 10.87 | 17.73 | 1.46 | 0.96 | 33.43 | 17.84 | 2.57 |
| 3200.00 | 12.35 | 21.77 | 10.64 | 17.84 | 1.47 | 0.97 | 32.91 | 17.81 | 2.70 |
| 3400.00 | 12.09 | 21.84 | 10.61 | 18.20 | 1.52 | 0.98 | 33.34 | 17.88 | 2.73 |
| 3500.00 | 12.00 | 21.75 | 10.43 | 17.93 | 1.51 | 0.98 | 33.57 | 17.63 | 2.89 |
| 3600.00 | 11.89 | 21.62 | 10.24 | 17.62 | 1.50 | 0.99 | 33.63 | 17.80 | 2.78 |
| 3800.00 | 11.68 | 21.57 | 10.12 | 17.40 | 1.52 | 0.99 | 33.53 | 17.82 | 2.91 |
| 4000.00 | 11.51 | 21.44 | 9.87 | 17.10 | 1.51 | 1.00 | 33.78 | 17.77 | 3.01 |
| 4200.00 | 11.36 | 21.39 | 9.75 | 16.86 | 1.52 | 1.00 | 33.67 | 17.67 | 2.96 |
| 4400.00 | 11.24 | 21.35 | 9.57 | 16.39 | 1.51 | 1.01 | 33.48 | 17.50 | 3.04 |
| 4500.00 | 11.08 | 21.33 | 9.53 | 16.36 | 1.54 | 1.01 | 33.53 | 17.62 | 3.12 |
| 4600.00 | 11.06 | 21.42 | 9.49 | 16.15 | 1.55 | 1.01 | 33.33 | 17.68 | 3.19 |
| 4800.00 | 10.90 | 21.23 | 9.20 | 15.40 | 1.52 | 1.02 | 33.45 | 17.59 | 3.25 |
| 5000.00 | 10.75 | 21.21 | 9.09 | 15.04 | 1.53 | 1.02 | 33.46 | 17.18 | 3.27 |
| 5200.00 | 10.64 | 21.03 | 8.71 | 14.21 | 1.49 | 1.02 | 33.61 | 17.24 | 3.34 |
| 5400.00 | 10.55 | 20.98 | 8.50 | 13.69 | 1.48 | 1.02 | 33.92 | 16.79 | 3.45 |
| 5500.00 | 10.50 | 20.92 | 8.35 | 13.36 | 1.47 | 1.02 | 33.27 | 17.75 | 3.44 |
| 5600.00 | 10.67 | 21.34 | 8.50 | 13.68 | 1.51 | 1.03 | 33.63 | 17.27 | 3.51 |
| 5700.00 | 10.57 | 21.11 | 8.18 | 13.01 | 1.46 | 1.03 | 33.71 | 17.19 | 3.51 |
| 5800.00 | 10.48 | 20.92 | 7.96 | 12.52 | 1.43 | 1.03 | 33.58 | 17.27 | 3.59 |
| 5900.00 | 10.40 | 20.86 | 7.76 | 12.12 | 1.41 | 1.03 | 33.69 | 17.15 | 3.70 |
| 6000.00 | 10.37 | 20.82 | 7.64 | 12.03 | 1.40 | 1.03 | 34.30 | 16.80 | 3.72 |
| 6500.00 | 10.12 | 20.52 | 6.68 | 10.59 | 1.30 | 1.04 | 33.96 | 16.82 | 4.00 |
| 7000.00 | 9.73 | 20.58 | 5.74 | 9.16 | 1.23 | 1.05 | 33.55 | 16.34 | 4.12 |
| 7500.00 | 8.78 | 20.45 | 5.07 | 7.72 | 1.19 | 1.04 | 32.63 | 15.47 | 4.72 |
| 8000.00 | 7.49 | 21.63 | 4.30 | 6.09 | 1.27 | 1.01 | 30.33 | 15.48 | 5.32 |

The RF switch uses an SPDT configuration with a frequency bandwidth of 9kHz to 8GHz. The RF switch integrates an internal electrostatic discharge (ESD) protection circuit, effectively protecting the RF ports. The switching logic of the RF switch is shown in the following table. For the AD9361 TX/RX switching configuration, please refer to the schematic for the actual connection details and corresponding control settings.

| LS | CTRL | RFC-RFC1 | RFC-RFC1 |
|---|---|---|---|
| 0 | 0 | OFF | ON |
| 0 | 1 | ON | OFF |
| 1 | 0 | ON | OFF |
| 1 | 1 | OFF | ON |

In addition, the RF front-end includes four LED indicators. A port setting value of 1 turns the corresponding LED on, while a setting value of 0 turns it off. The LED pin assignments are listed in the following table.

| LED | Pin Name | Pin Position |
|---|---|---|
| LED_RF_TX1 | IO_21P_35 | N15 |
| LED_RF_RX1 | IO_21N_35 | N16 |
| LED_RF_TX2 | IO_22P_35 | L14 |
| LED_RF_RX2 | IO_22N_35 | L15 |

* 2.13.2 AD9361 Control and Data Interfaces

The AD9361 digital interface consists of data ports and control ports. The data interface can be configured as either LVCMOS or LVDS. Since LVCMOS communication provides a lower data rate compared with LVDS, the development project provided by us uses the LVDS interface configuration as the default setting for the AD9361 data port.

The pin assignments are listed in the following table. For detailed connection information, please refer to the schematic.

| AD9361 Interface | Pin Name | Pin Position |
|---|---|---|
| AD9631_TX_P0 | IO_8P_34 | W14 |
| AD9631_TX_N0 | IO_8N_34 | Y14 |
| AD9631_TX_P1 | IO_5P_34 | T14 |
| AD9631_TX_N1 | IO_5N_34 | T15 |
| AD9631_TX_P2 | IO_4P_34 | V12 |
| AD9631_TX_N2 | IO_4N_34 | W13 |
| AD9631_TX_P3 | IO_10P_34 | V15 |
| AD9631_TX_N3 | IO_10N_34 | W15 |
| AD9631_TX_P4 | IO_6P_34 | P14 |
| AD9631_TX_N4 | IO_6N_34 | R14 |
| AD9631_TX_P5 | IO_9P_34 | T16 |
| AD9631_TX_N5 | IO_9N_34 | U17 |
| AD9631_TX_FRAME_P | IO_7P_34 | Y16 |
| AD9631_TX_FRAME_N | IO_7N_34 | Y17 |
| AD9631_FB_CLK_P | IO_11P_SRCC_34 | U14 |
| AD9631_FB_CLK_N | IO_11N_SRCC_34 | U15 |
| AD9631_RX_P0 | IO_21P_34 | V17 |
| AD9631_RX_N0 | IO_21N_34 | V18 |
| AD9631_RX_P1 | IO_17P_34 | Y18 |

| | | |
|---|---|---|
| AD9631_RX_N1 | IO_17N_34 | Y19 |
| AD9631_RX_P2 | IO_16P_34 | V20 |
| AD9631_RX_N2 | IO_16N_34 | W20 |
| AD9631_RX_P3 | IO_18P_34 | V16 |
| AD9631_RX_N3 | IO_18N_34 | W16 |
| AD9631_RX_P4 | IO_15P_34 | T20 |
| AD9631_RX_N4 | IO_15N_34 | U20 |
| AD9631_RX_P5 | IO_20P_34 | T17 |
| AD9631_RX_N5 | IO_20N_34 | R18 |
| AD9631_RX_FRAME_P | IO_19P_34 | R16 |
| AD9631_RX_FRAME_N | IO_19N_34 | R17 |
| AD9631_DATA_CLK_P | IO_13P_MRCC_34 | N18 |
| AD9631_DATA_CLK_N | IO_13N_MRCC_34 | P19 |
| AD9631_CLK_OUT | IO_14P_SRCC_34 | N20 |
| AD9631_SPI_CLK | IO_1P_34 | T11 |
| AD9631_SPI_nCS | IO_1N_34 | T10 |
| AD9631_SPI_DI | IO_2P_34 | T12 |
| AD9631_SPI_DO | IO_2N_34 | U12 |
| AD9631_nRST | IO_22N_34 | W19 |
| AD9631_ENABLE | IO_23P_34 | N17 |
| AD9631_EN_AGC | IO_23N_34 | P18 |
| AD9631_SYNC_IN | IO_24P_34 | P15 |
| AD9631_TXNRX | IO_24N_34 | P16 |
| AD9631_CTRL_OUT0 | IO_14P_SRCC_13 | Y9 |
| AD9631_CTRL_OUT1 | IO_16P_13 | W10 |
| AD9631_CTRL_OUT2 | IO_14N_SRCC_13 | Y8 |
| AD9631_CTRL_OUT3 | IO_15P_13 | V8 |
| AD9631_CTRL_OUT4 | IO_15N_13 | W8 |
| AD9631_CTRL_OUT5 | IO_16N_13 | W9 |
| AD9631_CTRL_OUT6 | IO_12N_MRCC_13 | U10 |
| AD9631_CTRL_OUT7 | IO_12P_MRCC_13 | T9 |
| AD9631_CTRL_IN0 | IO_11P_SRCC_13 | U7 |
| AD9631_CTRL_IN1 | IO_13N_MRCC_13 | Y6 |
| AD9631_CTRL_IN2 | IO_13P_MRCC_13 | Y7 |
| AD9631_CTRL_IN3 | IO_11N_SRCC_13 | V7 |

* 2.13.3 AD9361 Clock Circuit

The input clock source of the AD9361 uses a 40MHz VCTCXO with an accuracy of up to 0.5ppm. In addition, the board reserves an ADF4002BRUZ chip. For applications requiring higher clock accuracy, an external reference clock can be input through the RF header and adjusted using the ADF4002BRUZ. For detailed clock circuit information and usage instructions, please refer to the

schematic.

## 2.14 PPS and Clock Inputs

The HG61 Pro/HG63 Pro provides a PPS input and 10MHz clock input circuit. Both signals share the same MMCX interface for external input.

The onboard RC circuit, together with FPGA I/O control signals, is used to enable or disable the PPS and clock signal paths. In addition, the 10MHz reference clock signal is connected to the ADF4002 for clock synchronization and correction.

The PPS and clock signals are connected to the following FPGA pins:

| Signal Name | Pin Name | Pin Position |
|---|---|---|
| PPS-IN | IO_14P_SRCC_35 | J18 |
| 10M_FPGA | IO_12P_MRCC_34 | U18 |
| EN_10M_FPGA | IO_25_34 | T19 |
| EN_10M_CLKIN | IO_22P_34 | W18 |

## 2.15 GPS Module

The GPS module is integrated on the board and supports both GPS and BeiDou positioning functions. The module communicates through UART, allowing users to configure the module and read positioning data. In addition, it provides a PPS signal. The pin assignments of the GPS module are listed in the following table. For detailed connection information, please refer to the schematic.

| GPS Modue | Pin Name | Pin Position |
|---|---|---|
| GPS_UART_TXD | IO_16N_35 | G18 |
| GPS_UART_RXD | IO_17P_35 | J20 |
| GPS_nRESET | IO_16P_35 | G17 |
| GPS_PPS | IO_14N_35 | H18 |

## 2.16 I/O Expansion Ports

The board provides a 40-pin 2.54mm-pitch header for signal expansion. The following table lists the corresponding chip locations of the expansion signals. For detailed connection information, please refer to the schematic.

| IO Interface | Pin Name | Pin Position | Level Standards | IO Interface | Pin Name | Pin Position | Level Standards |
|---|---|---|---|---|---|---|---|
| 5 | IO_1P_35 | C20 | 3.3V | 6 | IO_15P_35 | F19 | 3.3V |
| 7 | IO_1N_35 | B20 | | 8 | IO_15N_35 | F20 | |
| 9 | IO_19P_35 | H15 | | 10 | IO_20P_35 | K14 | |
| 11 | IO_19N_35 | G15 | | 12 | IO_20N_35 | J14 | |
| 13 | IO_23P_35 | M14 | | 14 | IO_9P_35 | L19 | |
| 15 | IO_23N_35 | M15 | | 16 | IO_9N_35 | L20 | |
| 17 | IO_12N_35 | K18 | | 18 | IO_18N_35 | G20 | |
| 19 | IO_13N_35 | H17 | | 20 | IO_25_35 | J15 | |
| 21 | IO_20P_13 | Y12 | 1.8V | 22 | IO_21P_13 | V11 | 1.8V |
| 23 | IO_20N_13 | Y13 | | 24 | IO_21N_13 | V10 | |

## 2.17 User LEDs

The HG61 Pro/HG63 Pro provides two user-defined LEDs for application-specific functions. The LEDs are active high, meaning that a high-level signal turns the LED on, while a low-level signal turns it off. The LED pin assignments are listed in the following table. For detailed information, please refer to the schematic.

| LED Pin | Pin Name | Pin Position |
|---|---|---|
| LED1 | IO_0_35 | G14 |
| LED2 | IO_8N_35 | M18 |